SD C10M card series

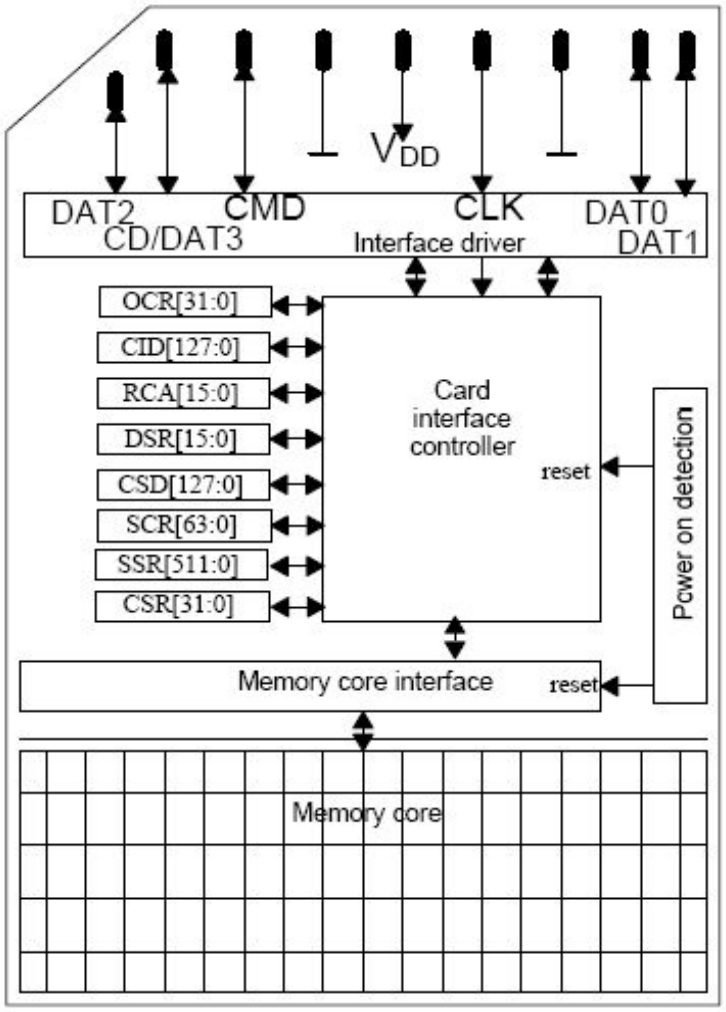
Description

Built with top-quality MLC NAND Flash chips, Transcend's Industrial use SDHC/SDXC Class 10 memory cards can endure operating temperatures ranging from -25°C to 85°C; setting a new standard in consistent, long-term performance even in the harshest conditions. Moreover, these cards offer high-speed Class 10 data transfer rates and extra large storage space to fully satisfy the demanding performance and capacity requirements of industrial applications.

Features

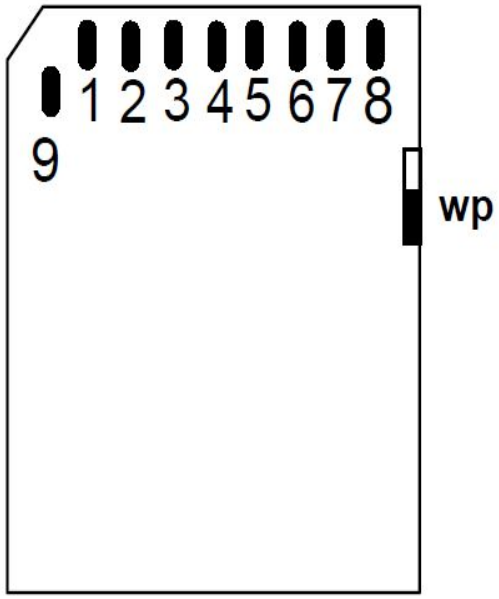
- Manufactured with brand-name MLC NAND Flash chips for extra long life and stability
- Class 10 speed rating guarantees fast and reliable write performance
- Compatible with SD Specification Ver. 3.01
- Mechanical Write Protection Switch
- Built-in ECC and Wear leveling
- Support ESD IEC 61000-4-2
- Support Early move and Read Retry

Architecture



Pin Definition

Pin No.	SD Mode		SPI Mode	
	Name	Description	Name	Description
1	CD/DAT3	Card Detect/Data Line [Bit3]	CS	Chip Select (neg true)
2	CMD	Command/Response	DI	Data In
3	V_{SS1}	Supply voltage ground	V_{SS}	Supply voltage ground
4	V_{DD}	Supply voltage	VDD	Supply voltage
5	CLK	Clock	SCLK	Clock
6	V_{SS2}	Supply voltage ground	V_{SS2}	Supply voltage ground
7	DAT0	Data Line [Bit0]	DO	Data out
8	DAT1	Data Line [Bit1]	RSV	Reserved
9	DAT2	Data Line [Bit2]	RSV	Reserved



Specifications

Physical Specification		
Form Factor		SD
SD specification		SD3.01
Dimensions (mm)	**Length**	32.00 ± 0.1
	Width	24.00 ± 0.1
	Height	2.10 ± 0.15

Performance				
Model P/N	**Sequential Read***	**Sequential Write***	**Random Read** (4KB QD32)*	**Random Write** (4KB QD32)*
TS8GSDHC10M	20	14	4.5	0.9
TS16GSDHC10M	21	17	6.8	1.1
TS32GSDHC10M	21	20	4.4	1.0
TS64GSDXC10M	20	18	3.7	0.8
TS128GSDXC10M	24	22	5.1	0.9

Note: Maximum transfer speed recorded
* 25 ℃ , 4GB DRAM, Windows® 7 with Transcend RDF5, benchmark utility Crystal DiskMark , copied file 1000MB, unit MB/s

Endurance		
TeraBytes Written (T.B.)	TS8GSDHC10M	15
	TS16GSDHC10M	30
	TS32GSDHC10M	60
	TS64GSDXC10M	120
	TS128GSDXC10M	240

*TBW is based on Transcend internal standard to calculate how much data can be written into the drive.
*1 TeraByte=1,000,000,000,000 bytes

Bus Mode/ Power Consumption		
		Value(Max.)
Default Mode (25MHz)	Read	100mA
	Write	100mA
	Idle	0.5mA
High Speed mode (50MHz)	Read	200mA
	Write	200mA
	Idle	0.5mA

Note: Power consumption is referred to Section 6.6.3 of the SDA Physical Layer Specification, Version 3.01

Environmental Specifications	
Operating Temperature	- 25℃ to 85℃
Storage Temperature	- 40℃ to 85℃
Durability	10.000 mating cycles
Drop test	1.5m free fall
Regulator	CE/FCC/BSMI

Product Description

1.Features

1.1 Lock Function

Support for password protected locking and unlocking of SD devices. It uses the LOCK/UNLOCK command(CMD42) which is available in SD command sets.

1.2 Built-in ECC Engine

In event of errors, the combined data allow the recovery of the original data. The number of errors that can be recovered depends on the algorithm used.

1.3 Wear-leveling

This function means the data are no longer tied to a single physical area, which can extend Card's life expectancy.

1.4 Read Retry

The function allows the read voltage to be dynamically adjusted such that read errors are decreased or even eliminated.

1.5 Early Move

The function provides a mechanism to avoid read disturbance. Built-in ECC is used to detect and correct data bit error. If error bits reaches the default threshold, the data will be moved to another good block and the original block should be erased to avoid un-correct error in advance.

2.Bus Topology

The SD Memory Card system defines two alternative communication protocols:SD and SPI. The host system can choose either one of modes. The card detects which mode is request by host when the reset command is received and expects all further communication to be in the same communication mode.

2.1 SD Bus

For more details, refer to Section 3.5.1 of the SDA Physical Layer Specification, Version 3.01.

2.2 SPI Bus

For more details, refer to Section 3.5.2 of the SDA Physical Layer Specification, Version 3.01.

3.SD card Register information

3.1 OCR register

The OCR register stores the VDD voltage profile of the card,refer to Section 5.1 of the SDA Physical Layer Specification, Version 3.01 for more information.

3.2 CID register

The Card Identification (CID) register is 128 bits wide. It contains the card identification information used during the card identification phase. Every individual flash card shall have a unique identification number. The structure of the CID register is defined in the following paragraphs:

Name	Field	Width	CID-slice
Manufacturer ID	MID	8	[127:120]
OEM/Application ID	OID	16	[119:104]
Product name	PNM	40	[103:64]
Product revision	PRV	8	[63:56]
Product serial number	PSN	32	[55:24]
reserved	--	4	[23:20]
Manufacturing date	MDT	12	[19:8]
CRC7 checksum	CRC	7	[7:1]
not used, always '1'	-	1	[0:0]

• MID
An 8-bit binary number that identifies the card manufacturer. The MID number is controlled, defined, and allocated to a SD Memory Card manufacturer by the SD-3C, LLC. This procedure is established to ensure uniqueness of the CID register.

• OID
A 2-character ASCII string that identifies the card OEM and/or the card contents (when used as a distribution media either on ROM or FLASH cards). The OID number is controlled, defined, and allocated to a SD Memory Card manufacturer by the SD-3C, LLC. This procedure is established to ensure uniqueness of the CID register.

•PNM
The product name is a string, 5 ASCII characters long.
PNM can be customized by Transcend

• PRV
The product revision is composed of two Binary Coded Decimal (BCD) digits, four bits each, representing an "n.m" revision number. The "n" is the most significant nibble and "m" is the least significant nibble.
As an example, the PRV binary value field for product revision "6.2" will be: 0110 0010

• PSN
The Serial Number is 32 bits of binary number.
PSN Number can be customized by Transcend

• MDT
The manufacturing date composed of two hexadecimal digits, one is 8 bit representing the year(y) and the other is four bits representing the month(m).
The "m" field [11:8] is the month code. 1 = January.
The "y" field [19:12] is the year code. 0 = 2000.
As an example, the binary value of the Date field for production date "April 2001" will be:
00000001 0100.
MDT can be customized by Transcend

• CRC
CRC7 checksum (7 bits).

3.3 CSD register

The following sections describe the CSD fields and the relevant data types for the standard and High Capacity SD Memory Card. CSD Version 1.0 is applied Capacity SD Memory Card and CSD Version is applied to 2.0 is applied to only the High Capacity SD Memory Card. The field name in parenthesis is set to fixed value and indicates that the host is not necessary to refer these fields. The fixed values enables host, which refers to these fields, to keep compatibility to CSD Version 1.0. The Cell Type field is coded as follows: R = readable, W(1) = writable once, W = multiple writable.

3.3.1 CSD Register Structure

CSD_STRUCTURE	CSD Structure version	Card capacity
0	CSD Version1.0	Standard Capacity
1	CSD Version2.0	High Capacity and Extended Capacity
2-3	reserved	

3.3.2 CSD Register Structure (CSD Version 1.0)

Name	Field	Width	Cell Type	CSD-slice
CSD structure	CSD_STRUCTURE	2	R	[127:126]
reserved	-	6	R	[125:120]
data read access-time-1	TAAC	8	R	[119:112]
data read access-time-2 in CLK cycles (NSAC*100)	NSAC	8	R	[111:104]
max. data transfer rate	TRAN_SPEED	8	R	[103:96]
card command classes	CCC	12	R	[95:84]
max. read data block length	READ_BL_LEN	4	R	[83:80]
partial blocks for read allowed	READ_BL_PARTIAL	1	R	[79:79]
write block misalignment	WRITE_BLK_MISALIGN	1	R	[78:78]
read block misalignment	READ_BLK_MISALIGN	1	R	[77:77]
DSR implemented	DSR_IMP	1	R	[76:76]
reserved	-	2	R	[75:74]
device size	C_SIZE	12	R	[73:62]
max. read current @VDD min	VDD_R_CURR_MIN	3	R	[61:59]
max. read current @VDD max	VDD_R_CURR_MAX	3	R	[58:56]
max. write current @VDD min	VDD_W_CURR_MIN	3	R	[55:53]
max. write current @VDD max	VDD_W_CURR_MAX	3	R	[52:50]

Name	Field	Width	Cell Type	CSD-slice
device size multiplier	C_SIZE_MULT	3	R	[49:47]
erase single block enable	ERASE_BLK_EN	1	R	[46:46]
erase sector size	SECTOR_SIZE	7	R	[45:39]
write protect group size	WP_GRP_SIZE	7	R	[38:32]
write protect group enable	WP_GRP_ENABLE	1	R	[31:31]
reserved for MultiMediaCard compatibility		2	R	[30:29]
write speed factor	R2W_FACTOR	3	R	[28:26]
max. write data block length	WRITE_BL_LEN	4	R	[25:22]
partial blocks for write allowed	WRITE_BL_PARTIAL	1	R	[21:21]
reserved	-	5	R	[20:16]
File format group	FILE_FORMAT_GRP	1	R/W(1)	[15:15]
copy flag (OTP)	COPY	1	R/W(1)	[14:14]
permanent write protection	PERM_WRITE_PROTECT	1	R/W(1)	[13:13]
temporary write protection	TMP_WRITE_PROTECT	1	R/W	[12:12]
File format	FILE_FORMAT	2	R/W(1)	[11:10]
reserved		2	R/W	[9:8]
CRC	CRC	7	R/W	[7:1]
not used, always'1'	-	1	-	[0:0]

3.3.3 CSD Register (CSD Version 2.0)

Name	Field	Width	Value	Cell Type	CSD-slice
CSD structure	CSD_STRUCTURE	2	01b	R	[127:126]
reserved	-	6	00 0000b	R	[125:120]
data read access-time	(TAAC)	8	0Eh	R	[119:112]
data read access-time in CLK cycles (NSAC*100)	(NSAC)	8	00h	R	[111:104]
max. data transfer rate	(TRAN_SPEED)	8	32h or 5Ah	R	[103:96]
card command classes	CCC	12	01x110110101b	R	[95:84]
max. read data block length	(READ_BL_LEN)	4	9	R	[83:80]
partial blocks for read allowed	(READ_BL_PARTIAL)	1	0	R	[79:79]
write block misalignment	(WRITE_BLK_MISALIGN)	1	0	R	[78:78]
read block misalignment	(READ_BLK_MISALIGN)	1	0	R	[77:77]
DSR implemented	DSR_IMP	1	x	R	[76:76]
reserved	-	6	00 0000b	R	[75:70]
device size	C_SIZE	22	00 xxxxh	R	[69:48]
reserved	-	1	0	R	[47:47]
erase single block enable	(ERASE_BLK_EN)	1	1	R	[46:46]
erase sector size	(SECTOR_SIZE)	7	7Fh	R	[45:39]
write protect group size	(WP_GRP_SIZE)	7	0000000b	R	[38:32]
write protect group enable	(WP_GRP_ENABLE)	1	0	R	[31:31]
reserved		2	00b	R	[30:29]
write speed factor	(R2W_FACTOR)	3	010b	R	[28:26]
max. write data block length	(WRITE_BL_LEN)	4	9	R	[25:22]
partial blocks for write allowed	(WRITE_BL_PARTIAL)	1	0	R	[21:21]
reserved	-	5	00000b	R	[20:16]
File format group	(FILE_FORMAT_GRP)	1	0	R	[15:15]
copy flag (OTP)	COPY	1	x	R/W(1)	[14:14]
permanent write protection	PERM_WRITE_PROTECT	1	x	R/W(1)	[13:13]
temporary write protection	TMP_WRITE_PROTECT	1	x	R/W	[12:12]
File format	(FILE_FORMAT)	2	00b	R	[11:10]
reserved	-	2	00b	R	[9:8]
CRC	CRC	7	xxxxxxxb	R/W	[7:1]
not used, always'1'	-	1	1	-	[0:0]

3.4 RCA register

The writable 16-bit relative card address register carries the card address that is published by the card during the card identification. Refer to Section 5.4 in the SDA Physical Layer Specification, Version 3.01 for more information.

3.5 SCR register

In addition to the CSD register, there is another configuration register named SD CARD configuration Register, SCR provide information on the SD memory card's special feature that were configured into the given card.Refer to Section 5.6 in the SDA Physical Layer Specification, Version 3.01 for more information.

3.6 SSR register

The SD status contains status bits that are related to the SD memory card proprietary features and may be used for future application-specific usage. The SD Status structure is described in Section 4.10.2 in the SDA Physical Layer Specification, Version 3.01.

Order information

Capacity	Transcend Part Number
8GB	TS8GSDHC10M
16GB	TS16GSDHC10M
32GB	TS32GSDHC10M
64GB	TS64GSDXC10M
128GB	TS128GSDXC10M

The technical information above is based on industry standard data and has been tested to be reliable. However, Transcend makes no warranty, either expressed or implied, as to its accuracy and assumes no liability in connection with the use of this product. Transcend reserves the right to make changes to the specifications at any time without prior notice. Due to the complexity and variety of industrial applications, for special applications and environments, it is strongly suggested to contact Transcend or its authorized resellers beforehand for compatibility confirmation

Transcend®
good memories start here

TAIWAN
E-mail: sales-tw@transcend-info.com

USA
Los Angeles:
E-mail: sales-us@transcend-info.com

Maryland:
E-mail: sales-us@transcend-info.com

Miami:
E-mail: sales-us@transcend-info.com

Silicon Valley:
E-mail: sales-us@transcend-info.com

GERMANY
E-mail: sales-de@transcend-info.com

THE NETHERLANDS
E-mail: sales-nl@transcend-info.com

United Kingdom
E-mail: sales-uk@transcend-info.com

JAPAN
E-mail: sales-jp@transcend-info.com

KOREA
E-mail: sales-kr@transcend-info.com

CHINA
E-mail: sales@transcendchina.com

HONG KONG
E-mail: sales-hk@transcend-info.com

Revision History

Version	Date	Note
1.0	2016/05/23	The 1st SD edition
1.1	2016/10/20	1.Revise pin definition of SPI mode 2.Modify 64GB performance 3.Add 8/128GB solution
1.2	2017/07/04	Modify TBW description
1.3	2017/07/06	1.Add 16/32GB solution